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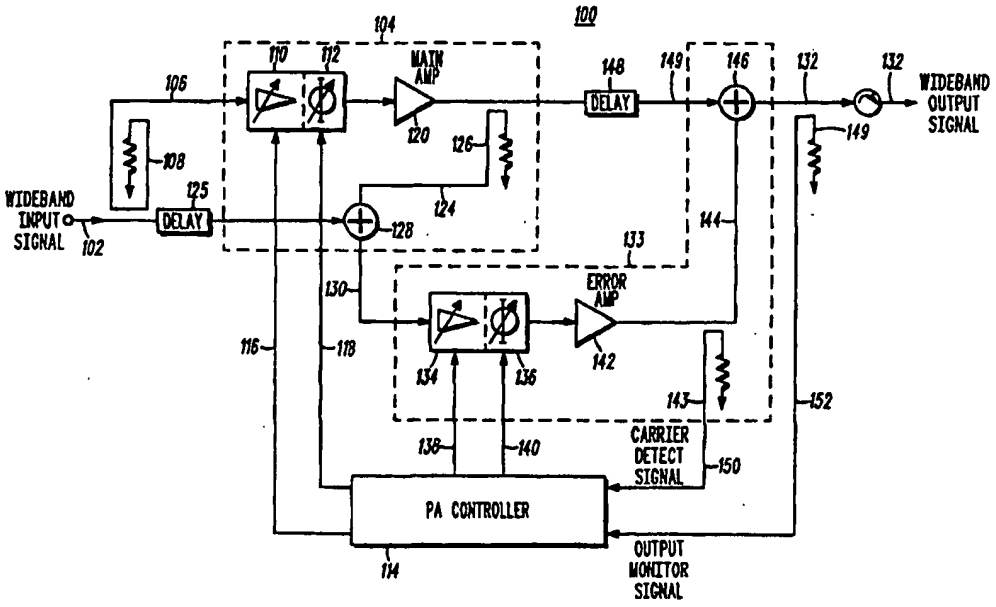


(57) Abstract

A control scheme is implemented to improve the transmission quality of a wideband output signal (132) transmitted by a power amplifier (100) in a wideband communication system. The scheme utilizes a control processor (502) to instruct a pair of digital-to-anallog converters (538, 542) to control carrier cancellation in a carrier cancellation block (104). The control processor (502) also instructs a different set of a digital-to-analog converters (546, 550) to control intermodulation product cancellation in an intermodulation product cancellation block (133). By optimizing cancellation of both the carrier and the intermodulation products, the linearity of the power amplifier (100) is improved.

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# Wideband Power Amplifier Control Systems

## Field of the Invention

The invention is generally related to control systems, and more particularly to control systems for use with power amplifiers utilized in code division multiple access (CDMA) communication systems.

## Background of the Invention

Code Division Multiple Access (CDMA) communication systems are well known. In a CDMA communication system, communication between two communication units (e.g., a central communication site and a mobile communication unit) is accomplished by spreading each transmitted signal over the frequency band of the communication channel with a unique user spreading code. Due to the spreading, transmitted signals are in the same frequency band of the communication channel and are separated only by unique user spreading codes. These unique user spreading codes preferably are orthogonal to one another such that the cross-correlation between the spreading codes is approximately zero. Consequently, when the user spreading codes are orthogonal to one another, the received signal can be correlated with a particular user spreading code such that only the desired user signal (related to the particular spreading code) is despread.

It will be appreciated by those skilled in the art that several different spreading codes exist which can be used to separate data signals from one another in a CDMA communication system. These

spreading codes include, but are not limited to, pseudo noise (PN) codes and Walsh codes. A Walsh code corresponds to a single row or column of the Hadamard matrix. For example, in a 64 channel CDMA spread spectrum system, particular mutually orthogonal Walsh codes can be selected from the set of 64 Walsh codes within a 64 by 64 Hadamard matrix. Also, a particular data signal can be separated from the other data signals by using a particular Walsh code to spread the particular data signal.

It will be further appreciated by those skilled in the art that spreading codes can be used to channel code data signals. The data signals are channel coded to improve performance of the communication system, and particularly radiotelephone communication systems, by enabling transmitted signals to better withstand the effects of various radiotelephone channel impairments, such as noise, fading, and jamming. Typically, channel coding reduces the probability of bit error, and/or reduces the required signal to noise ratio usually expressed as bit energy per noise density ($E_b/N_0$), to recover the signal at the cost of expending more bandwidth than would otherwise be necessary to transmit the data signal. For example, Walsh codes can be used to channel code a data signal prior to modulation of the data signal for subsequent transmission. Similarly psuedo-noise (PN) spreading codes can be used to channel code a data signal.

A typical CDMA transmission involves expanding the bandwidth of an information signal to produce a wideband signal, transmitting the wideband signal and recovering the desired information signal from the wideband signal by remapping the received spread spectrum into the original information signal's bandwidth. This series of bandwidth trades used in CDMA transmission allows the CDMA communication system to deliver a relatively error-free information signal in a noisy signal environment or communication channel. Transmission of the wideband signal to deliver the relatively error-free information signal in the noisy signal

environment requires the use of a linear power amplifier (LPA) so that the effects of typical amplifier "problems", for example interference generated outside of the channel bandwidth generated by intermodulation (IM) distortion, can be mitigated. Linearity, however, is usually achieved at the expense of very poor efficiency, especially at the high power levels required by CDMA communication systems. For example, Class A power amplifiers exhibit good linearity but draw constant current no matter what level the input signal may be. Consequently, a Class A power amplifier drawing high amounts of current to amplify small input signals (and sometimes no input signal) is very inefficient.

The implementation of feed-forward technology in power amplifiers is a excellent way to achieve good linearity. In typical feed-forward power amplifier implementations, a Class B biasing scheme is utilized. In Class B power amplifiers, efficiency is improved since the current draw of the power amplifier varies with the level of the input signal. This has the negative effect, however, of degrading linearity since the Class B power amplifier typically amplifies in its saturation region. As one of ordinary skill in the art will appreciate, an amplifier amplifying in its saturation region is highly non-linear and will thus produce undesired intermodulation products.

For a feed-forward power amplifier to achieve the desired linearity with adequate efficiency (i.e., acceptable for a given implementation), the gain and phase of both the main amplifier and the error amplifier need to be precisely controlled. To successfully obtain this precise control, a real-time controller which constantly optimizes the gain and phase of the main signal and the error signal for peak linearity is required. The prior art control techniques used to constantly optimize the gain and phase of both the main and error signals are complex for communication systems which typically utilize multiple narrowband carriers, such as analog communication systems like the Advanced Mobile Phone System (AMPS) communication

FIG. 5 generally depicts a block diagram of the power amplifier controller of FIG. 1 which provides control of a feed-forward power amplifier in accordance with the invention.

FIG. 6 generally depicts a signal exiting the detector of FIG. 5.

## Detailed Description of a Preferred Embodiment

Generally, a control scheme is implemented to improve the transmission quality of a wideband output signal transmitted by a Class B biased power amplifier in a wideband communication system. The scheme utilizes a control processor to instruct a pair of digital-to-analog converters to control carrier cancellation in a carrier cancellation block. The control processor also instructs a different set of digital-to-analog converters to control intermodulation product cancellation in an intermodulation product cancellation block. By optimizing cancellation of both the carrier and the intermodulation products, the linearity of the Class B biased power amplifier is improved.

More specifically, a power amplifier has as an input a wideband input signal and has as an output a wideband output signal, where the wideband output signal includes a carrier signal and undesired intermodulation products. The power amplifier monitors the wideband output signal to produce an output monitor signal which represents a replica of the wideband output signal, then downconverts the output monitor signal to a baseband signal which includes the carrier signal and the undesired intermodulation products. The power amplifier filters the baseband signal to substantially remove the carrier signal while leaving most of the undesired intermodulation products, and adjusts the power amplifier to mitigate the undesired intermodulation products in the wideband output signal.

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FIG. 1 generally depicts a power amplifier 100 for use in a CDMA communication system which may beneficially employ the feed-

forward control scheme in accordance with the invention. As shown in FIG. 1, a wideband input signal 102, which includes a carrier signal 200 as shown in FIG. 2, is input into a carrier cancellation block 104 which provides cancellation of the carrier signal 200 as described below. The carrier signal 200 is the signal which is transmitted, and provides information for a particular user. In the preferred embodiment, the carrier signal 200 is a modulated signal having a bandwidth of 1.25 MHz and is transmitted at radio frequencies ($RF_C$) in the frequency range 869-894 MHz. As one of ordinary skill in the art will appreciate, the control scheme in accordance with the invention may be adapted to suit transmission over any suitable frequency range.

Also entering the carrier cancellation block 104 is a replica signal 106 which is a result of coupling from the wideband input signal 102 via a coupler 108. The replica signal 106 is input into a main amplifier gain adjustment block 110 and a main amplifier phase adjustment block 112, where the gain and phase of the replica signal 106 is adjusted by a power amplifier (PA) controller 114 via the lines 116, 118 as will be described in detail hereinafter. The output of the phase adjust block 112 is input into a main amplifier 120 where high power amplification of the replica signal 106 occurs. The result of high power amplification by the amplifier 120 is the amplifier output signal 122, which as best seen in FIG. 3, includes both the carrier signal 200 and undesired intermodulation products 300 caused by the high power amplification.

At this point, a replica signal 124 of the amplifier output signal 122 is produced by the coupler 126. The replica signal 124, as is the wideband input signal 102 having a delay produced by the main amplifier delay block 125, is input into a summing node 128. Also input into the summing node 128 is a signal 127 which is a delayed replica of the wideband input signal 102. The delay produced by the delay block 125 is such that the signal 127 exiting the delay block 125 and the signal 124 arrive at the summing node 128 approximately simultaneously. In the preferred embodiment, the summing node 128

provides approximately 180° of phase difference between signals 124 and 127. The main amplifier gain adjustment block 110 will adjust the amplitude of the resulting signal 124 such that the amplitudes of the replica signal 124 and the signal 127 are approximately equal. Since the summing node 128 provides approximately 180° of phase difference, and the two signals have approximately equal amplitudes, the carrier signal 200 as shown in FIG. 2 and FIG. 3 will effectively be canceled when the replica signal 124 is summed with the signal 127 at the summing node 128. Consequently, the resulting output of the summing node 128 is a carrier-canceled signal 130 which has a substantial portion of the carrier signal 200 removed. The carrier-canceled signal 130 is represented as shown in FIG. 4.

Since the carrier-canceled signal 130 has a substantial portion of the carrier signal 200 removed (when near ideal control is accomplished), the same procedure as described above for the carrier signal 200 can be repeated to mitigate the undesired intermodulation products 300 in the wideband output signal 132. This is accomplished as follows. The carrier-canceled signal 130 is input into an intermodulation product cancellation block 133, which comprises an error amplifier gain adjustment block 134 and an error amplifier phase adjustment block 136. The gain adjust block 134 and the phase adjust block 136 adjust the gain and phase of the node output signal 130. Control is performed by the power amplifier controller 114 via the lines 138, 140 as will be described in detail hereinafter. The output of the phase adjust block 136 is input into an error amplifier 142 which amplifies the adjusted version of the carrier-canceled signal 130. The result of error amplification by the error amplifier 142 is the intermodulation (IM) canceled signal 144, which is similar to the carrier-canceled signal 130 depicted in FIG. 4 (but for gain/phase adjustment and amplification). The IM-canceled signal 144 is summed, via a summing node 146, with a signal 149 which is a delayed version of the amplifier output signal 122. The delay produced by a delay block

148 is such that the IM-canceled signal 144 and the signal 149 arrive at the summing node 146 approximately simultaneously. The summing node provides 180° of phase difference, and thus the undesired intermodulation products 300 which are contained in both the IM-canceled signal 144 and signal 149 will be substantially canceled. Consequently, instead of having the wideband output signal 132 include the undesired intermodulation products 300 (which it would if the amplifier output signal 122 as shown in FIG. 3 were the output signal), the resulting wideband output signal 132 has the undesired intermodulation products 300 substantially canceled. Thus, the wideband output signal 132 looks similar to the wideband input signal 102 (see FIG. 2), having only the carrier signal 200.

As stated above, cancellation of the carrier signal 200 in the carrier cancellation block 104 and cancellation of the undesired intermodulation products 300 in the intermodulation product cancellation block 133 occurs because of the approximately equal amplitude levels and the approximately 180° phase difference of the summed signals in each of the cancellation blocks 104 and 133. In the ideal scenario, perfect amplitude matching and perfect 180° phase difference would result in perfect cancellation; i.e., no carrier signal 200 in carrier-canceled signal 130 and no undesired intermodulation products 300 in wideband output signal 132. However, due to imperfect delays introduced by delay blocks 126 and 146, component variations, etc., the desirous perfect amplitude matching and perfect 180° phase difference is difficult to achieve without a control scheme. In the power amplifier 100 depicted in FIG. 1, the gain adjustment blocks 110 and 134 and the phase adjustment blocks 112, 136 are constantly adjusted in an attempt to achieve the perfect amplitude matching/180° phase difference required to achieve a wideband output signal 132 which has the minimum amount of the undesired intermodulation products 300.

FIG. 5 generally depicts a block diagram of the power amplifier controller 114 which provides control of the feed-forward power amplifier 100 implemented in a manner to maintain improved amplifier linearity without sacrificing amplifier efficiency in accordance with the invention. As shown in FIG. 1 and FIG. 5, a carrier detect signal 150 is coupled from the IM-canceled signal 144 via the coupler 143, and represents a replica of the IM-canceled signal 144 exiting the error amplifier 142. The carrier detect signal 150, which is input into the power amplifier controller 114, is utilized to improve carrier cancellation in carrier-canceled signal 130. Also, an output monitor signal 152 is coupled from the wideband output signal 132 via the coupler 149, and represents a replica of the output wideband signal 132. The output monitor signal 152 is also input into the power amplifier controller 114, and is utilized as a "feed-back" signal by the power amplifier controller 114 to adjust gain adjustment blocks 110 and 134 and phase adjustment blocks 112 and 136 in accordance with the invention.

Recalling that perfect 180° phase difference (to result in perfect cancellation of the undesired intermodulation products 300) is difficult to achieve, the output monitor signal 152, a replica of the wideband output signal 132, will have some amount of undesired intermodulation products 300 thereon. To control the power amplifier 100 such that near-perfect 180° phase difference is achieved, the power amplifier controller 114 incrementally adjusts the gain adjustment blocks 110 and 134 and phase adjustment blocks 112 and 136. The circuitry of FIG. 5 performs such control.

Referring to FIG. 5, the control process begins when a control processor 502 commands a RF switch 504, via the line 506, to switch to the output monitor signal 152. In the preferred embodiment, the control processor 502 is a Motorola 68HC11 processor. Continuing, with the RF switch 504 so switched, the output monitor signal 152 is input into a RF mixer 508. The RF mixer 508 also has as an input the output

of a voltage controlled oscillator (VCO) 510 which is controlled by a digital-to-analog converter (D/A) 512 via the line 514. The output of the VCO 510 is amplified by an amplifier 516, while the input is lowpass filtered by lowpass filter (LPF) 518. To begin the control process, the control processor 502 sweeps the D/A converter 512, via a line 520, from its minimum output value to its maximum output value. While this sweeping occurs, the RF mixer 508 mixes the output monitor signal 152 down to a baseband signal 509 which is bandpass filtered by notch/bandpass filter 522. The output of the filter 522 is amplified by the amplifier 524, and input into a detector 526 which detects the root mean square (RMS) level of the resulting filtered baseband signal 529. The signal 528 exiting the detector 526 is shown in FIG. 6.

Referring to FIG. 6, the signal 528 exiting the detector 526 is shown to have a maximum 602, a minimum 604 and a maximum value 606. As the VCO 510 starts its sweep, the baseband signal 509 will be significantly outside of the band of the filter 522. In the preferred embodiment, the filter 522 has a notch portion 521 from 0 Hz to approximately 900 kHz to provide notch filtering. The filter 522 also has a bandpass portion 523 from approximately 1 MHz to approximately 5 MHz to provide bandpass filtering. Since the signal exiting the RF mixer 508 is outside the band of the filter 522, the RMS level of the output of the filter 522 will be high. As the VCO begins to tune the baseband signal exiting the RF mixer 508 into the band of the filter 522, the RMS level of the output of the filter 522 will begin to enter the notch portion 521 of the filter 522, and will thus begin to fall. When the baseband signal is exactly centered at (i.e., at 0 Hz of filter 522), the RMS level of the output of the filter 522 will be at the minimum 604 as designated in FIG. 6. Again, as the VCO 510 continues its sweep, the RMS level of the output of the filter 522 will begin to rise to its maximum value 606. The maximum values 602, 606 are essentially identical, and are due to the double side-bands (RF-LO and RF+LO) caused by the mixing process.

Before the VCO 510 is swept, the control processor 502 commands a multiplexer (MUX) 530, via the line 532, to switch to the output of the detector 526. As such, the signal 528 is routed to an analog-to-digital (A/D) converter 534 where the signal 528 is digitized, and input into the control processor 502 via the line 536. In the preferred embodiment, the MUX 530 and the A/D converter 534 reside on the Motorola 68HC11 processor. Continuing, the control processor 502 monitors the digitized version of the signal 528, determines the maximum 602 (or 606; either can be used) and the minimum 604 of the digitized version of the signal 528, and correlates the maximum 602 and the minimum 604 with the control values output (by control processor 502) to the D/A converter 512 necessary to achieve the maximum 602 and the minimum 604. The corresponding control values, labeled $C_{max}$ and $C_{min}$ for convenience, are stored in memory internal to the control processor 502.

At this point, adjustment of the main amplifier gain adjustment block 110 and the main amplifier phase adjustment block 112 to provide improved carrier cancellation in carrier-canceled signal 130 is performed. Stated generally, control signals are generated by the control processor (502) based on a characteristic related to the IM-canceled signal (144) and the wideband output signal (132). The control process starts when the control processor 502 commands the RF switch 504, via the line 506, to switch to the carrier detect signal 150. At substantially the same time, the control processor 502 applies the control value $C_{max}$ to the D/A converter 512. Recall that the carrier detect signal 150 is a replica of IM-canceled signal 144 which has the carrier signal 200 substantially removed by the carrier cancellation block 104. However, since a small portion of the carrier signal 200 will remain on the IM-canceled signal 144, its replica - the carrier detect signal 150 - will also have a small portion of the carrier signal 200 thereon. As such, the control processor 502 sweeps the D/A converter 538, via the line 540, through a limited tuning range until the

minimum 604 is found in the signal 528. The corresponding control value required to produce the minimum 604 is output by the control processor 502, via the line 540, to the D/A 538, which subsequently outputs a control value to the main amplifier gain adjustment block 110 via the line 116. When adjustment of the main amplifier gain adjustment block 110 is completed, the above process is repeated for the main amplifier phase adjustment block 112 using the D/A converter 542 under control of the control processor 502 via the line 544.

The above steps are substantially repeated to perform adjustment of the error amplifier gain adjustment block 134 and the error amplifier phase adjustment block 136 to provide improved intermodulation product cancellation in IM-canceled signal 144. The process starts when the control processor 502 commands the RF switch 504, via the line 506, to switch to the output monitor signal 152. At substantially the same time, the control processor 502 applies the control value $C_{min}$ to the D/A converter 512. The control processor 502 will sweep the D/A converter 546, via the line 548, through a limited tuning range until the minimum 604 is found in the signal 528. The corresponding control value required to produce the minimum 604 is output by the control processor 502, via the line 548, to the D/A 546, which subsequently outputs a control value to the error amplifier gain adjustment block 134 via the line 138. When adjustment of the error amplifier gain adjustment block 134 is completed, the process is repeated for the error amplifier phase adjustment block 136 using the D/A converter 550 under control of the control processor 502 via the line 552.

The feed-forward power amplifier 100 will amplify in its saturation region as do most Class B biased amplifiers, but the control scheme implemented in accordance with the invention will correct for a substantial portion of the undesired intermodulation products. Since intermodulation products are manifested as interference in bands other than the transmission band, the mitigation of intermodulation products leads directly to a mitigation of out-of-band interference.

Since capacity in CDMA communication systems increases as interference decreases, the control scheme in accordance with the invention leads to an increase in CDMA system capacity. Additionally, the control scheme is implemented in a CDMA communication system in a simple manner (only a single controller is required to control both carrier cancellation and IM product cancellation) to maintain improved amplifier linearity without sacrificing amplifier efficiency, and vice versa.

While the invention has been particularly shown and described with reference to a particular embodiment, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention. The corresponding structures, materials, acts and equivalents of all means or step plus function elements in the claims below are intended to include any structure, material, or acts for performing the functions in combination with other claimed elements as specifically claimed.

## Claims

1. A power amplifier controller for use in a power amplifier compatible with a wideband communication system, the power amplifier amplifying a wideband input signal and producing a wideband output signal, the power amplifier controller comprising:

a control processor having as outputs a plurality of control signals;

a voltage controlled oscillator (VCO);

a first digital-to-analog (D/A) converter coupled to the control processor and the VCO;

a mixer having as inputs an output of the VCO and a signal related to the wideband output signal;

a filter coupled to an output of the mixer;

a detector responsive to the filter and outputting a signal representing an output level of the filter;

second and third digital-to-analog (D/A) converters coupled to the control processor and respectively coupled to first and second gain adjustment blocks in the power amplifier; and

fourth and fifth digital-to-analog (D/A) converters coupled to the control processor and respectively coupled to first and second phase adjustment blocks in the power amplifier.

2. The controller of claim 1 wherein the plurality of control signals further comprises a plurality of digital control signal.

3. The controller of claim 1 wherein the filter further provides both bandpass filtering and notch filtering.

4. The controller of claim 1 wherein the control processor is responsive to the signal representing an output level of the filter.

5. The controller of claim 1 wherein the wideband communication system further comprises a code division multiple access (CDMA) communication system.

6. A power amplifier for use in a wideband communication system, the power amplifier amplifying a wideband input signal having a carrier signal wherein the result of amplification is the generation of undesired intermodulation (IM) products, the power amplifier comprising:

a carrier cancellation block, having as an input the wideband input signal, for substantially canceling the carrier signal from the wideband input signal to produce as an output a carrier-canceled signal, the carrier cancellation block also having as an output an amplifier output signal;

an IM product cancellation block, responsive to the carrier-canceled signal and a version of the amplifier output signal, for substantially canceling the IM products from the carrier-canceled signal to produce as an output an IM-canceled signal, the IM-canceled signal being summed with the version of the amplifier output signal to produce a wideband output signal; and

a power amplifier controller, coupled to both the carrier cancellation block and the IM product cancellation block, for adjusting components of both blocks to mitigate the IM products in the wideband output signal.

7. A method of controlling a power amplifier compatible with a wideband communication system, the power amplifier amplifying a wideband input signal having a carrier signal wherein the result of amplification is the generation of undesired intermodulation (IM) products, the power amplifier producing a wideband output signal, the method comprising the steps of:

switching a switch, having as an input an output monitor signal and a carrier detect signal, to output the output monitor signal;

tuning, via a plurality of control signals output by a control processor to a first digital-to-analog converter, a voltage controlled oscillator (VCO) to produce a plurality of signals having frequencies substantially near a frequency of the output monitor signal;

mixing the plurality of signals with the output monitor signal to produce a baseband signal;

filtering the baseband signal to produce a signal having maximum and minimum values;

detecting the signal having maximum and minimum values;

determining, in the control processor, which control signals produced the maximum value and the minimum value;

setting an output of the VCO based on the determined control signals; and

adjusting components in the power amplifier to mitigate the IM products in the wideband output signal.

8. The method of claim 7, wherein the step of adjusting components in the power amplifier further comprises the steps of:

adjusting components in a carrier cancellation block; and

adjusting components in an intermodulation (IM) cancellation block.

9. The method of claim 8, wherein the step of adjusting components in the carrier cancellation block further comprises the steps of:

switching the switch to output the carrier detect signal;

setting an output of the VCO based on the control signal determined to produce the maximum value;

sweeping, via control signals output by the control processor, a second digital-to-analog converter which controls a gain adjustment block in the carrier cancellation block to produce a signal having maximum and minimum values;

determining, in the control processor, which control signal produced the minimum value;

setting the second digital-to-analog converter to the control signal which produced the minimum value;

sweeping, via control signals output by the control processor, a third digital-to-analog converter which controls a phase adjustment block in the carrier cancellation block to produce a signal having maximum and minimum values;

determining, in the control processor, which control signal produced the minimum value; and

setting the third digital-to-analog converter to the control signal which produced the minimum value.

10. The method of claim 8, wherein the step of adjusting components in the intermodulation (IM) cancellation block further comprises the steps of:

switching the switch to output the output monitor signal;

setting an output of the VCO based on the control signal determined to produce the minimum value;

sweeping, via control signals output by the control processor, a fourth digital-to-analog converter which controls a gain adjustment block in the IM cancellation block to produce a signal having maximum and minimum values;

determining, in the control processor, which control signal produced the minimum value;

setting the fourth digital-to-analog converter to the control signal which produced the minimum value;

sweeping, via control signals output by the control processor, a fifth digital-to-analog converter which controls a phase adjustment block in the IM cancellation block to produce a signal having maximum and minimum values;

determining, in the control processor, which control signal produced the minimum value; and

setting the fifth digital-to-analog converter to the control signal which produced the minimum value.

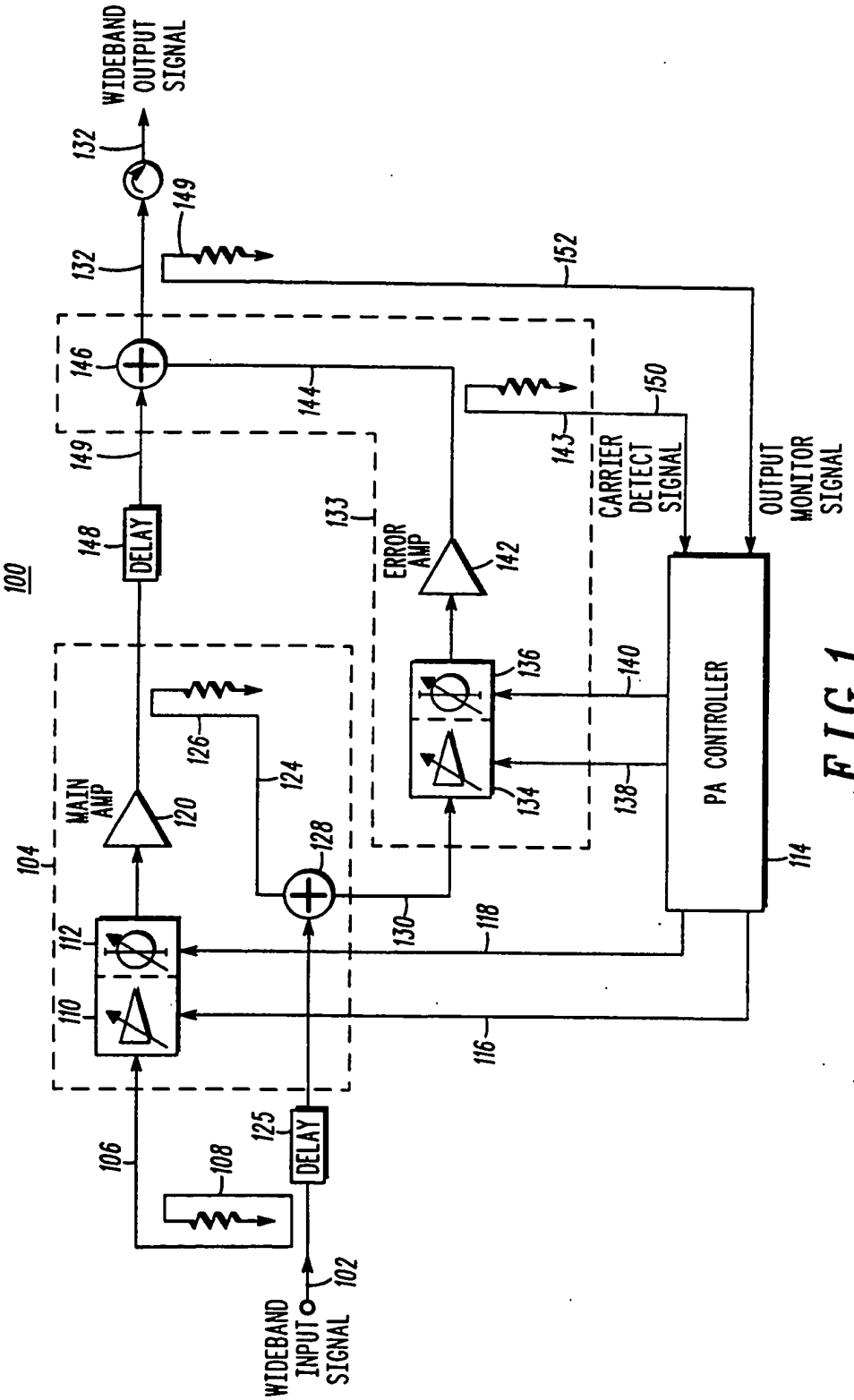

WIDEBAND OUTPUT SIGNAL
132
149
152
146
144
150
143
CARRIER DETECT SIGNAL
OUTPUT MONITOR SIGNAL
148
DELAY
133
ERROR AMP
142
100
136
140
126
124
MAIN AMP
120
134
138
PA CONTROLLER
104
128
114
112
130
118
110
116
106
108
125
DELAY
WIDEBAND INPUT SIGNAL
102

FIG.1

FIG.2

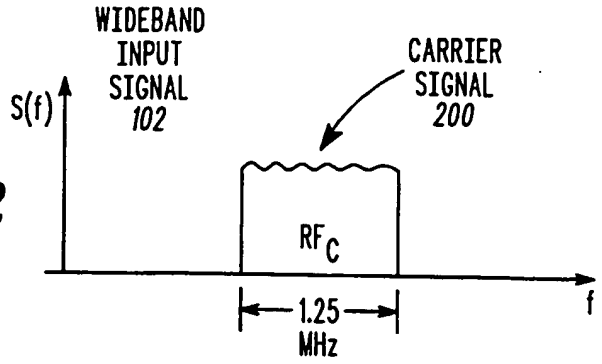



FIG.3

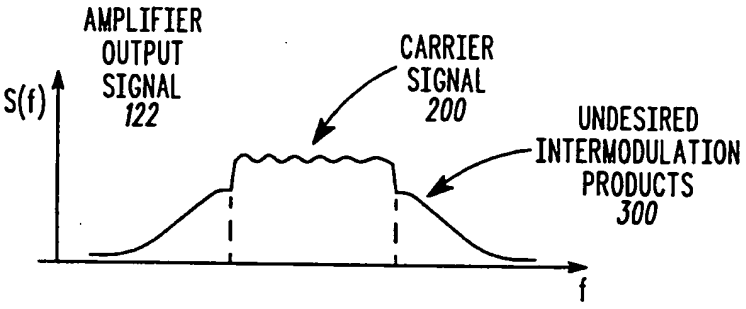



FIG.4

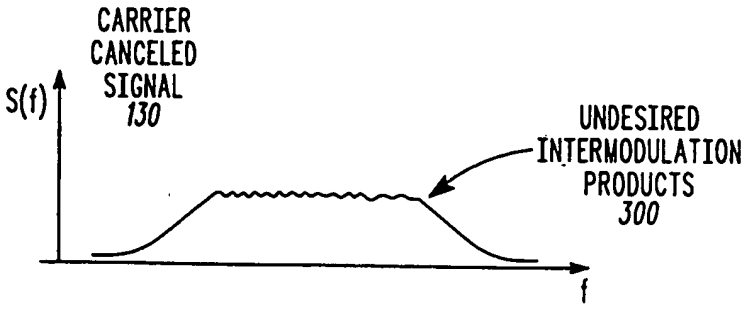
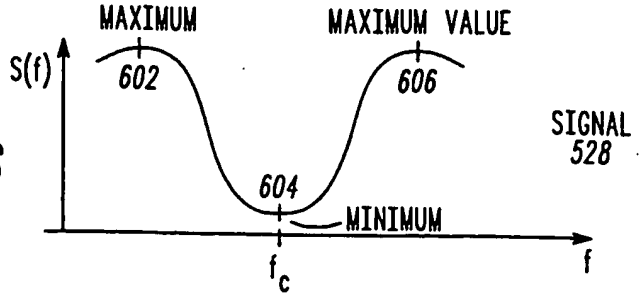



FIG.6



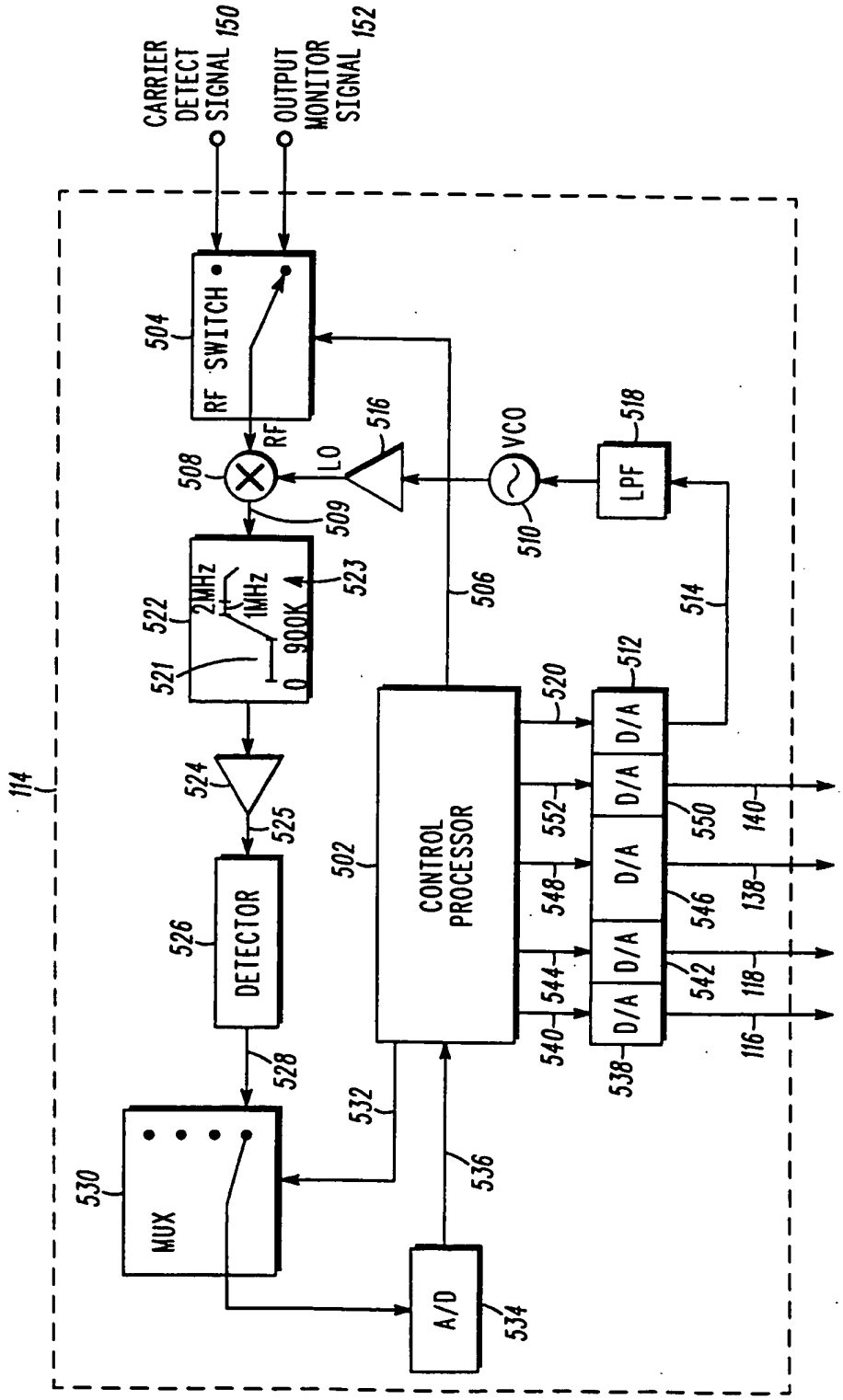

CARRIER DETECT SIGNAL 150
OUTPUT MONITOR SIGNAL 152
RF SWITCH 504
RF
LO 516
VCO 518
LPF
508
509
510
2MHz
1MHz
900K
0
522
523
521
506
514
524
525
114
CONTROL PROCESSOR 502
D/A 512
520
552
548
544
540
538
550
546
542
140
138
118
116
DETECTOR 526
528
532
MUX 530
536
A/D 534

FIG.5

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/10827

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) :H03F 1/32
US CL :330/151
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 330/151, 149; 375/297; 455/63

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
none

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
APS
Search terms: IM, intermodulation, distortion, products, feedforward, feed forward, CDMA, code division multiple access

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | US, A, 4,885,551 (Myer) 05 December 1989. Note Fig. 3 and col. 4, line 4 to col. 5, line 52. | 1-10 |
| X, P | US, A, 5,489,875 (Cavers) 06 February 1996. See Fig. 4 and col. 7, lines 11-31. | 6 |

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

| | | | |
|---|---|---|---|
| * | Special categories of cited documents: | "T" | later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention |
| "A" | document defining the general state of the art which is not considered to be of particular relevance | "X" | document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone |
| "E" | earlier document published on or after the international filing date | "Y" | document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art |
| "L" | document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) | "&" | document member of the same patent family |
| "O" | document referring to an oral disclosure, use, exhibition or other means | | |
| "P" | document published prior to the international filing date but later than the priority date claimed | | |

| | |
|---|---|
| Date of the actual completion of the international search<br>23 JULY 1996 | Date of mailing of the international search report<br>29 JUL 1996 |
| Name and mailing address of the ISA/US<br>Commissioner of Patents and Trademarks<br>Box PCT<br>Washington, D.C. 20231<br>Facsimile No. (703) 305-3230 | Authorized officer<br>James B. Mullins<br>Telephone No. (703) 308-4912 |

Form PCT/ISA/210 (second sheet)(July 1992)*